IN THE CLAIMS

Please cancel claims 11 and 12 without prejudice or disclaimer.

Applicants note that claim 3 is not amended to overcome prior art but to written in independent form. The amendment made to claim 3 is not narrowing in scope and therefore no prosecution history estoppel arises from the amendment to claim 3. *Festo Corp v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 U.S.P.Q.2d 1705, 1711-1712 (2002); 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2000). Further, the amendment made to claim 3 was not made for a substantial reason related to patentability and therefore no prosecution history estoppel arises from such amendments. *See Festo Corp.*, 62 U.S.P.Q.2d 1705 at 1707 (2002); *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 41 U.S.P.Q.2d 1865, 1873 (U.S. 1997).

Claim 1 (previously amended) A method for fabricating a memory device on a silicon substrate, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area, wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate; and

(c) strengthening the interface by providing a nitrification process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area.

Claim 2 (original) The method of claim 1 further comprising:

(d) depositing a layer of type-1 polysilicon in both the core area and periphery area of the memory device;

(e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and

(f) removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device.

Claim 3 (currently amended) [The method of claim 2] A method for fabricating a memory device on a silicon substrate, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area, wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate;

(c) strengthening the interface by providing a nitrification process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area;

(d) depositing a layer of type-1 polysilicon in both the core area and periphery area of the memory device;

(e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and

(f) removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device, wherein step (f) further includes removing approximately half the layer of type-1 polysilicon from the periphery area of the memory device.

Claim 4 (original) The method of claim 3 further comprising:

(g) depositing a layer of type-2 polysilicon in both the core and periphery areas of the memory area.

Claims 5-9 (~~withdrawn~~) canceled

Claim 10 (previously amended) A method for fabricating a memory device on a silicon substrate, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area, wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate;

(c) strengthening the interface by providing a nitrification process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area;

(d) depositing a layer of type-1 polysilicon in both the core area and periphery area of the memory device;

(e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and

(f) removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device.

Claims 11-12 (canceled)